Subject: LINEAR & DIGITAL IC APPLICATIONS

(1) ***OBJECTIVES AND RELEVANCE***

This course introduces the basic concepts logic gates which is the most useful for designing the IC Technology in engineering discipline. The emphasis of this course is laid on the basic analysis of digital circuits.

(2) ***SCOPE***

The scope of this subject is to provide an insight into designing the DTl, TTL ECL circuits which are useful in digital devices. This concept is more useful in further applications of minimizing the complexity of logic circuits.

(3) ***PREREQUISITES***

This subject recommends continuous practice of various simple arithmetic operations like addition, subtraction. It needs requisite knowledge about assuming and designing the logic circuits. How to reduce the size and complexity of the digital circuits.

(4.1) ***SYLLABUS - JNTU***

UNIT-I

Operational Amplifier: Ideal and practical Op-amp, OP-Amp characteristics, DC and AC characteristics, Features of 741 Op-amp, Modes of Operation-Inverting, Non-inverting, Differential, Instrumentation amplifier, AC amplifier, Differentiators and Integrators, Comparators, Schmitt Trigger, Introduction to voltage regulators, Features of 723 Regulator, Three Terminal Voltage Regulators.

UNIT – II

OP- AMP, IC-555 & IC-565 Applications: Introduction to Active Filters, Characteristics of Band pass, Band reject and all pass filters, Analysis of 1st order LPF & HPF Butterworth Filters, Waveform Generators- Triangular, Sawtooth, Square wave, IC555 Timer- functional diagram, Monostable and Astable operations, Applications, IC565 PLL- Block Schematic, Description of individual blocks, Applications

UNIT – III

Data Converters: Introduction, Basic DAC techniques, Different types of DACs-weighted resistor DAC, R-2R ladder DAC, inverted R-2R DAC, Different types of ADCs - parallel comparator type ADC, counter type ADC, successive approximation ADC and dual slope ADC, DAC and ADC Specifications

UNIT – IV

Digital Integrated Circuits: Classification of Integrated Circuits, Comparison of Various Logic Families, CMOS Transmission Gate, IC Interfacing- TTL Driving CMOS & CMOS Driving TTL, Combinational Logic ICs- Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs- Code Converters, Decoders, Demultiplexers, LED & LCD Decoders with Drivers, Encoders, Priority Encoders, multiplexers, Priority Generators/Checkers, Parallel Binary Adder/Subtractor, Magnitude Comparators.

UNIT – V

SYLLABUSSequential Logic IC's and Memories: Familiarity with commonly available 74XX & CMOS 40XX Series ICs- All types of Flip-Flops, Synchronous Counters, Decade Counters, Shift Registers.
Memories-ROM Architecture, Types of ROMS & Applications, RAM Architecture, Static & Dynamic RAMs.

(4.2) ***SYLLABUS - GATE***

UNIT I
Simple op-amp circuits

UNIT II
Function generators and wave-shaping circuits, 555 Timers

UNIT III
ADCs, DACs

UNIT IV
Digital IC families (DTL, TTL, ECL, MOS, CMOS), code converters, multiplexers, decoders

UNIT V
Flip-flops, counters and shift-registers, PROMs, Semiconductor memories

(4.3) ***SYLLABUS - IES***

UNIT I
Simple op-amp circuits

UNIT II
Function generators and wave-shaping circuits, 555 Timers

UNIT III
ADCs, DACs

UNIT IV
Digital IC families (DTL, TTL, ECL, MOS, CMOS), code converters, multiplexers, decoders

UNIT V
Flip-flops, counters and shift-registers, PROMs, Semiconductor memories

(5) ***SUGGESTED BOOKS***

TEXT BOOKS:

REFERENCES:

(6) ***WEBSITES***

1. www.ieee.org
2. www.2dix.com
3. www.xillinx.com
4. www.cdac.com
5. www.vlsi.edu
6. www.vlsi.iitkgp.ernet.in
7. www.educypedia.be/electronic/digital.com
8. www.iitb.ac.in
9. www.iitm.ac.in
10. www.iitr.ac.in
11. www.iitg.ernet.in
12. www.bits-pilani.ac.in
13. www.metorgraphics.com
14. www.vlsi-reasearch.com
15. www.iisc.ernet.in
16. www.samsung.com
17. www.vedaiit.com

(7) *EXPERT DETAILS*

The Expert Details which have been mentioned below are only a few of the eminent ones known Internationally, Nationally and Locally. There are a few others known as well.

INTERNATIONAL

1. **Prof. K Subbarangaiah** is Director of VEDA IIT, Hyderabad

NATIONAL

1. Dr.K. LAL KISHORE, Ph.D., MIEEE, FIETE, MISTE, MISHM, JNTU, Hyderabad
2. Mr .Sundaram, AGM, CAD R&D, ECIL, Hyderabad..
3. Mr. Rajendra naik, Asst Prof, Dept of ECE, Osmania University, Hyderabad.

REGIONAL

1. Dr. N.S.Murthy, Professor and Head Dept. of ECE, REC,Warangal - 506004 (India) email: nsm@recw.ernet.in
2. ***S.G Vinayaka Prasad, Sr. App. Engineer, Silicon Micro Systems***
3. DR. M. Madhavi Latha, JNTU, Hyderabad
4. Dr. Sarat Chandra Babu, Centre Head C-DAC, Hyderabad email: Sarat_chandra@hotmail.com

(8) *JOURNALS*

INTERNATIONAL

1. IEEE transactions on DIGITAL DESIGNS
2. IEEE proceedings circuits, devices and systems
3. International journal of circuit designs and applications
4. IEEE transactions on IC design
5. VSI vision

NATIONAL

1. DIGITAL DESGIN MAGAZINE
2. JOURNAL FOR DIGITAL SYSTEMS
3. IBM system magazine

(9) *SUBJECT (LESSON) PLAN*

Topic Name	No. of classes	Text books
UNIT I: OPERATIONAL AMPLIFIER		
Ideal and practical Op-amp	01	T3, T2
OP-Amp characteristics	01	T3, T2
DC and AC characteristics, Features of 741 Op-amp	03	T3, T2
Modes of Operation-Inverting, Non-inverting	02	T3, T2
Differential, Instrumentation amplifier, AC amplifier	02	T3, T2
Differentiators and Integrators	01	
Comparators, Schmitt Trigger	02	T3, T2
Introduction to voltage regulators, Features of 723 Regulator	02	T3, T2
Introduction to voltage regulators, Features of 723 Regulator	01	T3, T2
	15	
UNIT II: OP- AMP, IC-555 & IC-565 APPLICATIONS		
Introduction to Active Filters,	01	T3, T2
Characteristics of Band pass	01	T3, T2
Band reject and all pass filters	02	T3, T2
Analysis of 1st order LPF & HPF Butterworth Filters	03	T3, T2
Waveform Generators- Triangular, Saw tooth, Square wave	03	T3, T2
IC555 Timer- functional diagram	01	T3, R5
Monostable and Astable operations, Applications	02	T3, R5
IC565 PLL- Block Schematic, Description of individual blocks, Applications	02	T3, R5
	15	
UNIT III: DATA CONVERTERS		
Introduction, Basic DAC techniques	02	T3, R5
Different types of DACs-weighted resistor DAC	01	T3, R5
R-2R ladder DAC, inverted R-2R DAC	02	T3, R5
Different types of ADCs - parallel comparator type ADC	01	T3, R5
counter type ADC	01	T3, R5

successive approximation ADC and dual slope ADC	02	T3, R5
DAC and ADC Specifications	01	T3, R5
	10	
UNIT IV: DIGITAL INTEGRATED CIRCUITS		
Classification of Integrated Circuits	01	T3, R5
Comparison of Various Logic Families	02	T3, R5
CMOS Transmission Gate	01	T3, R5
IC Interfacing- TTL Driving CMOS & CMOS Driving TTL	02	T3, R5
Combinational Logic ICs- Specifications and Applications of TTL-74XX & CMOS 40XX Series ICs	02	T3, R5
Code Converters, Decoders, Demultiplexers	03	T3, R5
LED & LCD Decoders with Drivers	01	T3, R5
Encoders, Priority Encoders	02	T3, R5
multiplexers, Priority Generators/Checkers	02	T3, R5
Parallel Binary Adder/Subtractor	02	T3, R5
Magnitude Comparators	01	T3, R5
	19	
UNIT V: SEQUENTIAL LOGIC IC'S AND MEMORIES		
Familiarity with commonly available 74XX & CMOS 40XX Series ICs	01	T3, R5
All types of Flip-Flops	01	T3, R5
Synchronous Counters, Decade Counters	02	T3, R5
Shift Registers	02	T3, R5
Memories-ROM Architecture	01	T3, R5
Types of ROMS & Applications	01	T3, R5
RAM Architecture	01	T3, R5
Static & Dynamic RAMs	02	T3, R5
Total No. of Classes	**11**	
Total No. of Classes	**70**	

(10) *QUESTION BANK-* JNTU

Unit I:

1. Mention the advantages of integrated circuits.

2. write down the various processes used to fabricate IC's using silicon planar
3. technology.

4. What is the purpose of oxidation?
5. Why aluminum is preferred for metallization?

6. Define an operational amplifier. Mention the characteristics of an ideal op-amp. Define input offset voltage
7. What are the applications of current sources?
8. Define sensitivity. Mention the advantages of Wilson current source

9. What is a current mirror? Explain the working of a wilder current source
10. What is slew rate? Discuss the methods of improving slew rate.

11. What is an Active load? Explain the CE amplifier with active load
12. Explain pole zero compensation and frequency compensation in op-amp.
13. Define band gap reference? Explain in detail about the reference circuit
14. Briefly explain the method of using constant current bias for increasing CMRR in differential?
15. Explain the operation of a Schmitt trigger circuit
16. Explain the working of full precision rectifier?
17. Define ripple rejection with respect to voltage regulators.

18. With circuit diagram discuss the following applications of op-amp
19. Voltage to current converter(ii)Precision rectifier

20. Explain the operation of a Schmitt trigger circuit

21. Explain the working of full precision rectifier

22. Explain the internal structure of voltage regulator IC 723. Also draw a low
23. voltage Regulator circuit using IC 723andexplain its operation.

24. Explain the following terms in an OP-AMP. Bias current

    a. Thermal drift
    b. Input offset voltage and current
    c. Thermal drift

25. Explain the frequency compensation techniques of OP-AMP

26. Draw the circuit of a symmetrical emitter coupled differential amplifier and derive for CMRR.

27. Write a technical note on frequency response characteristics of differential amplifier. State the importance of frequency compensation

28. What is t instrumentation amplifier? What are the required parameters of an instrumentation amplifier? Explain the working of instrumentation amplifier
29. with neat circuit diagram

30. Explain various DC and AC characteristics of an op.amp. Distinguish between ideal and practical characteristics
31. With circuit and waveforms explain the application of OPAMP as (1)Integrator (2) Voltage series Feedback Compensation

Unit II:

1. Why active filters are preferred?
2. What is meant by cut off frequency of a high pass filter and how it is found out in a first order high pass filter
3. List the applications of 555 timer in monostable mode of operation
4. Define 555 IC?
5. List the basic blocks of IC 555 timer?
6. Define VCO.
7. What does u mean by PLL?
8. List the applications of 565 PLL
9. Define lock range.
10. Define capture range
11. Define pull-in time

Unit III:

1. List the broad classification of ADCs
2. List out the direct type ADCs
3. List out some integrating type converters
4. What is integrating type converter
5. Explain in brief the principle of operation of successive Approximation ADC
6. What are the main advantages of integrating type ADCs
7. What is the main drawback of a dual-slop ADC?
8. Define conversion time.
9. Define accuracy of converter
10. Explain in brief stability of a converter

Unit IV:

1. Explain how PROM, EPROM and EEPROM technologies differ from each other.
2. Design CMOS transistor circuit for 2-input AND gate.
3. Explain sourcing current of TTL output?
4. Which of the parameters decide the fan-out and how?
5. Explain sinking current of TTL output?
6. Explain the term Voltage levels for logic ‘1’ & logic ‘0’ with reference to TTL gate?
7. Explain the DC Noise margin with reference to TTL gate?
8. Explain Low-state unit load with reference to TTL gate?
9. Explain High-state fan-out with reference to TTL gate?
10. Explain the use of Package?

Unit V:

1. Define static RAM
2. Define dynamic RAM
3. Classify types of ROMs
4. Applications of ROMS
5. What is the difference between latch& Flip-Flop, Explain with logic diagram.
6. Explain any one application of SR latch.
7. What is race around condition? how it is avoided?
8. How synchronous counters differ from asynchronous counters?
9. List counter applications.
10. State various applications of counters.

Assignment Questions:

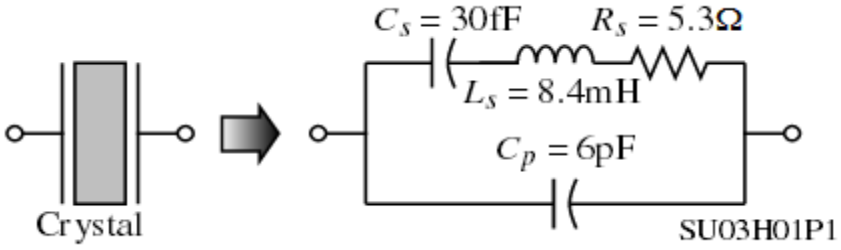
Assignment I

Issued date: 28/8/2017

Submit date: 1/9/2017

SET-I

1. Explain the Characteristics of 741 IC Along with the Applications? (Essay type)
2. Calculate the LOOP GAINS for 565 IC With different Frequencies?(Problem analysis)
3. Enhance the Op-Amp Performance by Improving Gain and CMRR Ratio?(Research based)
4. Solve for and evaluate the series and parallel resonance frequencies of the crystal Whose model is shown? It is suggested to make appropriate assumptions as the exact frequencies are difficult to achieve? (Problem analysis)



SET-II

1. What is the importance of 555 Timer in IC &Explain how it Works as a Multivibrator? (essay type)
2. Design an R-2R DAC for the input of 1110 and calculate output voltage?(Problem analysis)
3. Design Mobile Phone Detector Using LM358?(Project based)
4. Design a linear PLL in simulink?(Program based)

Assignment II

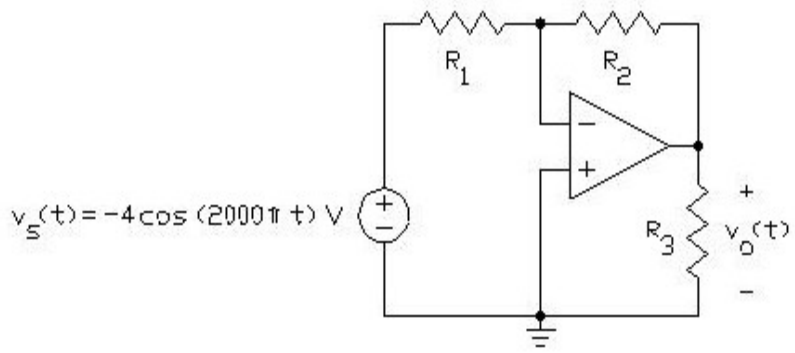
Issued date:

1/11/2017

Submit date: 7/11/2017

SET-III

1. Explain the briefly about different types of Combinational circuits?(Essay type)
2. Design a divide by 20 counter using IC 7490?(project based)
3. Analyze OP-AMP circuit using MATLAB?(Program based)



4. Design of OP-AMP using CMOS technology & its application?(research type)

SET-IV

1. Using the method of flip-flop conversion carry out the following conversions. (problem analysis)
   i) S-R to T
   ii) J-K to D
   iii) T to D
2. Realize the following expression using 74×151 IC f(Y) = AB + BC + AC. (Problem analysis)
3. Design a Remote Control Light by using 555 Timer?(Project based)
4. To write a VHDL Program to generate a 1010 sequence detector? (Program based)

Code No: 07A4EC02 **Set No. 1**

II B.Tech II Semester Regular Examinations, Apr/May 2009
LINEAR AND DIGITAL IC APPLICATIONS
(Common to Electrical & Electronic Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) With help of a block diagram explain the basic building blocks of an Op-amp.
   (b) What does the term 'balanced output' mean in an Op-amp?
   (c) List the parameters that should be considered for AC and DC application. [6+2+8]

2. (a) What is a clipper? With circuit diagram, explain the operation of positive and negative clippers.
   (b) Describe the principle of operation of a precision half wave rectifier with wave forms. [10+6]

3. (a) Derive the expression for frequency of oscillation of a RC phase shift oscillator and explain the operation of the circuit.
   (b) Design a second order low pass filter at a high cut off frequency of 1 KHz. Derive the transfer function of the above filter. [8+8]

4. (a) Give the block diagram of NE 565 PLL and explain the role of each block. Make circuit connections to track the incoming signal and explain its operations.
   (b) With neat sketches, explain the following terms:
      i. Lock-in-range.
      ii. Capture range
      iii. Pull-in time.
   (c) Sketch the capture transient and explain why it is generated before locking? [10+3+3]

5. (a) Differentiate between D-A and A- D CONVERTERS.
   (b) Explain D/A converter with R and 2R resistors. [8+8]

6. (a) Define logic family and explain
   (b) Sketch TTL OR Gate and explain its working
   (c) Sketch TTL AND Gate and explain its working. [4+6+6]

7. Design 8 - bit adder using 7482 . [16]

8. (a) What is the major difference between digital and analog PLLs?

Code No: 07A4EC02 **Set No. 1**

(b) Explain the frequency multiplier using IC PLL. [8+8]

Code No: 07A4EC02 **Set No. 2**

II B.Tech II Semester Regular Examinations, Apr/May 2009
LINEAR AND DIGITAL IC APPLICATIONS
(Common to Electrical & Electronic Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Derive closed loop voltage gain, input resistance, output resistance and bandwidth for inverting amplifier with feedback arrangement. [10+6]
   (b) Explain any one of the frequency compensation technique in connection with Op-amp.
2. (a) Explain the operation of Zero crossing detector.
   (b) Briefly mention the disadvantages of using Zero crossing detector and how it is overcome in Schmitt Trigger?
   (c) Draw a circuit using Op-amp which can work as adder (inverted and non-inverted) and explain how it works. [4+4+8]
3. (a) Classify the filters and explain the characteristics of each one of them.
   (b) Draw the first order low-pass Butterworth filter and analyze the same by deriving the gain and phase angle equation. [8+8]
4. (a) Describe the 555 time Monostable multivibrator applications in
      i. Frequency Modulation.
      ii. Pulse Width Modulation.
   (b) Describe
      i. Pulse Position Modulation (PPM) and
      ii. FSK generator
      using 555 timer astable multivibrator. [4+4+8]
5. (a) The basic step of a 16-bit DAC is 10.3 mV. If 0000000011111111 represents 0V, what output is produced if the input is 1111111111011011?
   (b) Calculate the values of the LSB, MSB and full scale output for an 32bit DAC for the 0 to 20V. [8+8]
6. A 74LS TTL gate drives four 74HC CMOS gates. Minimum Vcc is 4.75 V. Determine the minimum value of pull-up resistor for interfacing these devices.(VOL(max)=0.4V, IOL=8mA and IIL=-1microA
   (a) Explain TTL inverter with open collector output.
   (b) Compare various logic families
   (c) Differentiate bipolar IC and MOS IC. [4+4+4+4]

7. Design and explain the following

   (a) Basic comparator operation

   (b) Logic diagram for comparison of 2- bit binary numbers. [8+8]

8. Explain 74194 four bit bidirectional universal shift register with block diagram and timing diagram. . [16]

Code No: 07A4EC02 **Set No. 3**

II B.Tech II Semester Regular Examinations, Apr/May 2009
LINEAR AND DIGITAL IC APPLICATIONS
(Common to Electrical & Electronic Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Define slew rate and derive the expression for it. List causes of the slew rate and explain its significance in applications.
   (b) Explain the difference between slew rate and transient response. [10+6]
2. (a) What is Gyrator circuit? Explain its operation with a neat circuit diagram.
   (b) What is a sample and hold circuit? Why is it needed? With neat circuit diagram, describe the operation of an Op-amp based sample and hold circuit. [6+10]
3. (a) Derive the expression for frequency of oscillation of a RC phase shift oscillator and explain the operation of the circuit.
   (b) Design a second order low pass filter at a high cut off frequency of 1 KHz. Derive the transfer function of the above filter. [8+8]
4. (a) List the application of IC 565PLL and briefly describe the role of the PLL in any of that application.
   (b) Referring to the circuit shown in figure 4b determine the free running output, lock range and the capture range . [8+8]

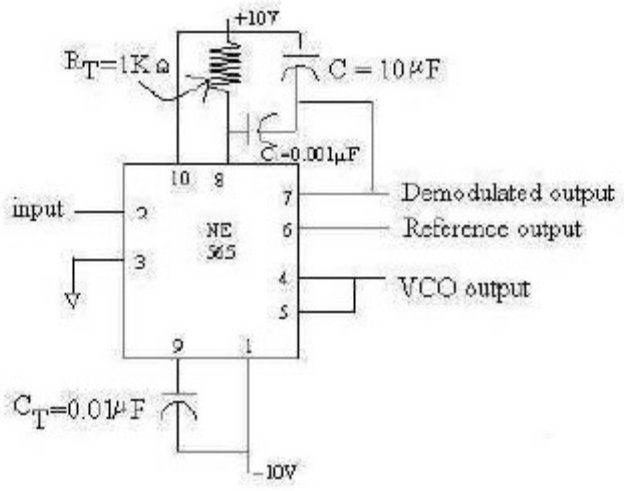


Figure 4b

Code No: 07A4EC02 **Set No. 3**

5. (a) Compare different A/D converters for their merits and demerits.
   (b) Give the schematic circuit diagram of a successive approximation type A/D converter and explain the operations of this system. [8+8]
6. (a) Explain the classification of integrated circuits
   (b) Sketch TTL NAND Gate and explain its working
   (c) Sketch TTL NOR Gate and explain its working. [4+6+6]
7. Explain Decimal - to - BCD priority Encoder. [16]
8. Expand 32K X 1 RAMs to form 32K X 4 RAM . [16]

Code No: 07A4EC02 **Set No. 4**

II B.Tech II Semester Regular Examinations, Apr/May 2009
LINEAR AND DIGITAL IC APPLICATIONS
(Common to Electrical & Electronic Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What are the three factors that affect the electrical parameters of an Op-amp.
   (b) Derive the expression for CMRR for the first stage differential amplifier. [8+8]
2. (a) Sketch the circuit of a logarithmic amplifier using one Op-amp and explain its operation. State its application.
   (b) What is a sample and hold circuit? Why is it needed? Draw a sample and hold circuit and explain its operation. [8+8]
3. (a) Derive the transfer function, gain and phase angle for second order high pass active filter.
   (b) Explain how Q, upper cutoff frequency and lower cutoff frequency is determined in Band pass filter. [8+8]
4. (a) Define the terms Lock range and Capture range
   (b) Calculate the frequency f_O, lock range $\triangle f_L$ and capture range $\triangle f_C$ of 565 PLL if R_T=10KΩ, C_T= 0.01μF, C=10μF. Shown in figure 4b. [6+10]

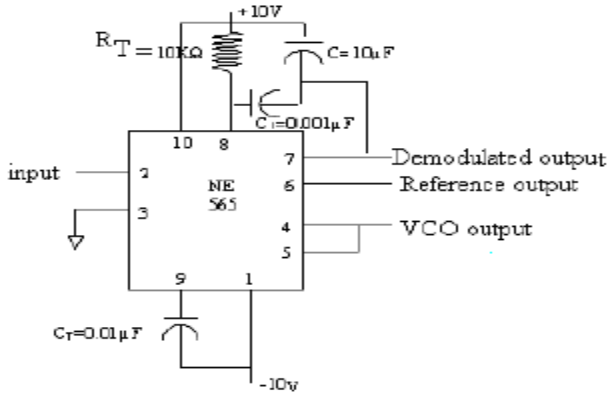


Figure 4b

5. Explain different types A/D and D/A converters. [16]
6. Specify the following parameters for 74H CMOS:

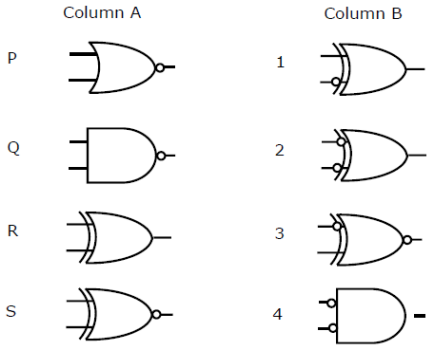
(a) $V_{OL(max)}$
(b) $V_{OH(min)}$
(c) $V_{IL(max)}$
(d) $V_{IH(min)}$ [4+4+4+4]

7. (a) Explain Decimal to BCD Encoder
(b) Explain application of an encoder using a keyboard encoder. [8+8]

8. (a) Find a modulo-6 gray code using k-Map & design the corresponding counter.
(b) Compare synchronous & Asynchronous. [8+8]

GATE 2010

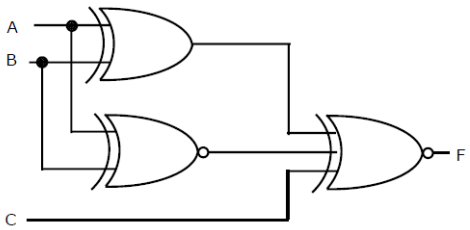
1. Match the logic ga5tes in **Column A** with their equivalents in **Column B.**



(A) P–2, Q-4, R-1, S-3 (B) P-4, Q-2, R-1, S-3

(C) P–2, Q-4, R-3, S-1 (D) P-4, Q-2, R-3, S-1

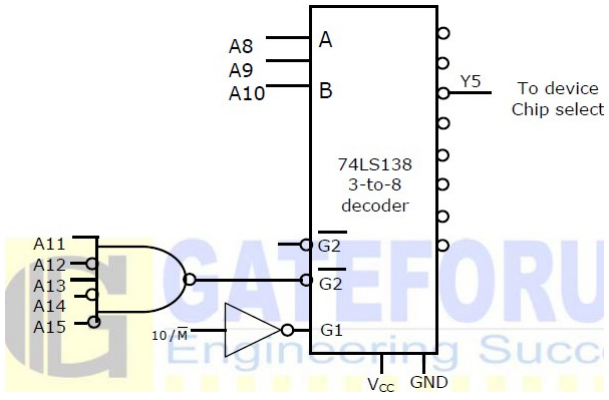
2. For the output F to be 1 in the logic circuit shown, the input combination should be



(A) A = 1, B= 1. C = 0 (B) A = 1, B= 0,C = 0

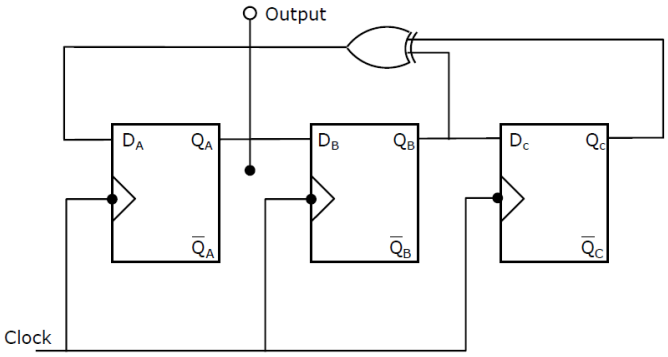
(C) A = 0, B= 1. C = 0 (D) A = 0, B= 0, C = 1

3. In the circuit shown, the device connected to Y5 can have address in the range



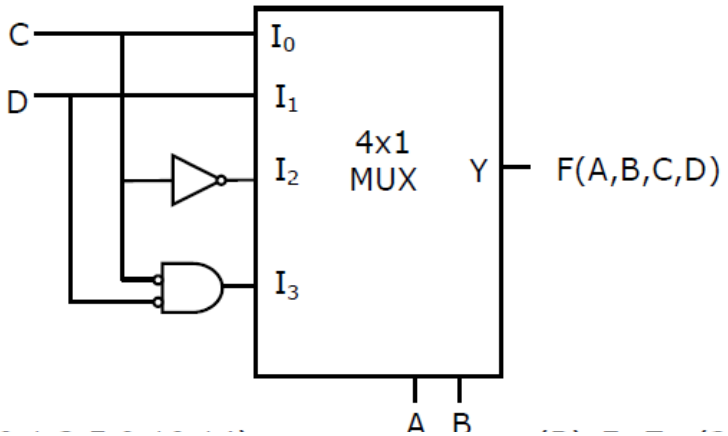
(A) 2000 - 20FF (B) 2D00 – 2DFF (C) 2E00 – 2EFF (D) FD00 - FDFF

4. Assuming that flip-flops are in reset condition initially, the count sequence observed at QA in the circuit shown is



(A) 0010111... (B) 0001011... (C) 0101111... (D) 0110100...

5. The Boolean function realized by the logic circuit shown is

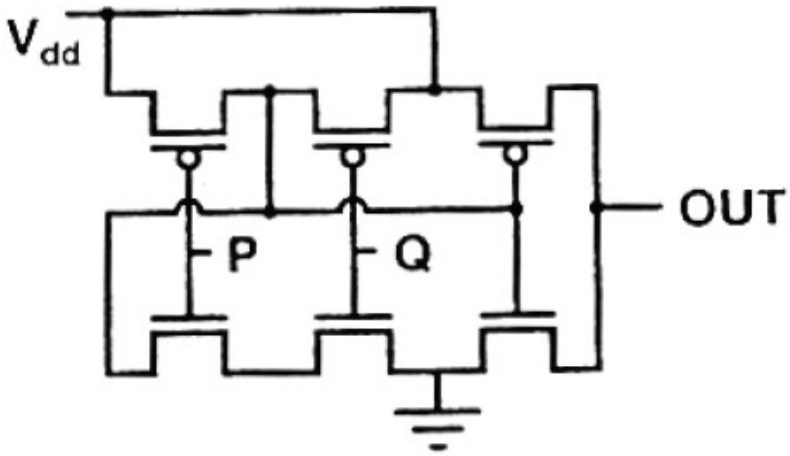


(A) F=Σm(0,1,3,5,9,10,14) (B) F=Σm(2,3,5,7,8,12,13)

(C) F=Σm(1,2,4,5,11,14,15) (D) F=Σm(2,3,5,7,8,9,12)

GATE 2008

6. The logic function implemented by the following circuit at the terminal OUT is



A) P NOR Q B) P NAND Q C) P OR Q D) P AND Q

7 .The two numbers represented in signed 2's complement form are P=11101101 and Q=11100110.If Q is subtracted from P,the value obtained in signed 2's complement form is

A) 100000111 B) 00000111 C) 11111001 D) 111111001

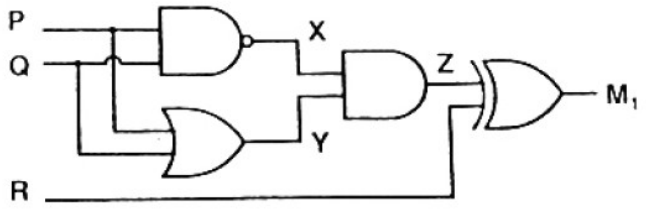
8. Which of the following Boolean Expression correctly represents the relation between P,Q,R and Mi

(a) M = (P OR Q) XOR R

(b) M_1 = (P AND Q) XOR R

(c) M = (P NOR Q) XOR R

(d) M_1 = (P XOR Q) XOR R



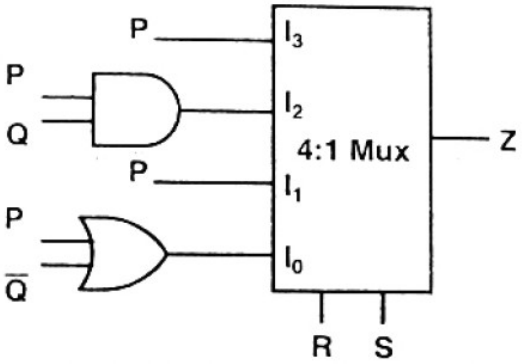
9. For the circuit shown in the following figure, Io –I3 are inputs to the 4:1 Multiplexer (MSB) are control bits. The output Z can be represented by

(a) $PQ + P\bar{Q}S + \bar{Q}\bar{R}\bar{S}$

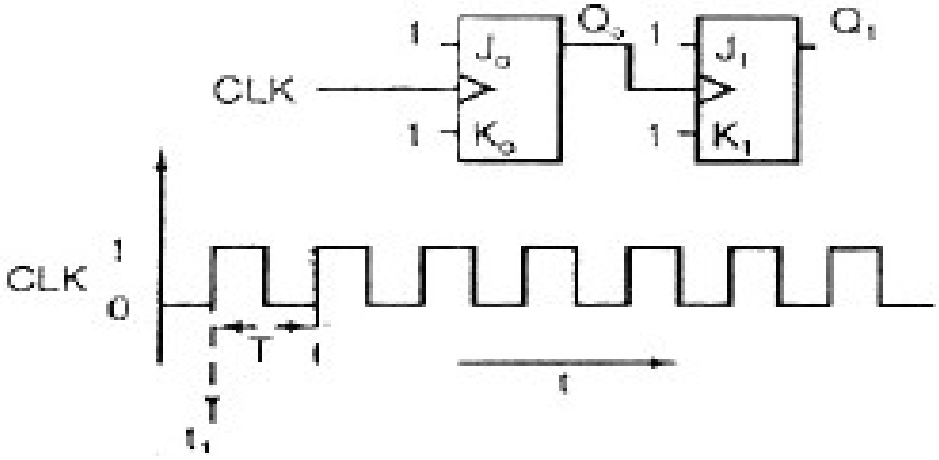
(b) $P\bar{Q} + PQ\bar{R} + \bar{P}\bar{Q}\bar{S}$

(c) $P\bar{Q}\bar{R} + \bar{P}QR + PQRS + \bar{Q}\bar{R}\bar{S}$

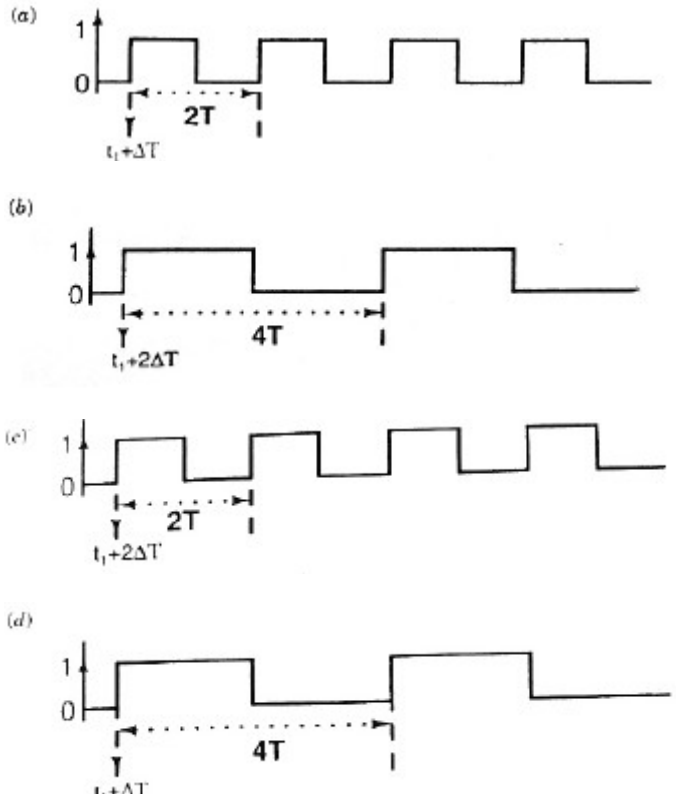
(d) $PQ\bar{R} + PQR\bar{S} - P\bar{Q}\bar{R}S + \bar{Q}R\bar{S}$



10.For each of the Positive edge-Triggered J-K flipflop used in the following figure, the propagation delay is ΔT.

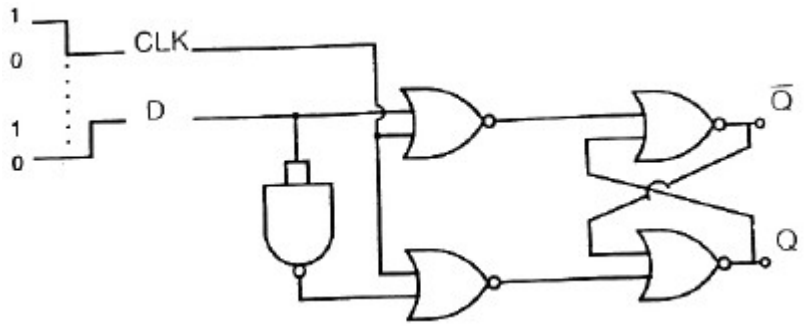


Which of the waveforms correctly represents the output at Q1?



11. For the circuit shown in the figure D has a transition from 0 to 1 after CLK changes from 1 to 0.

Assume gate delays to be negligible.



Which of the following statement is true?

A) Q goes to 1 at the CLK transition and stays at 1

B) Q goes to 0 at the CLK transition and stays at 0

C) Q goes to 1 at the CLK transition and goes to 0 when D goes to 1

D) Q goes to 0 at the CLK transition and goes to 1 when D goes to 1

GATE 2007

12. X=01110 and Y=11001 are two 5-bit binary numbers represented in Two's complement format. The sum of X and Y represented in Two's complement format using 6 bit is

A) 100111 B) 001000 C) 000111 D) 101001

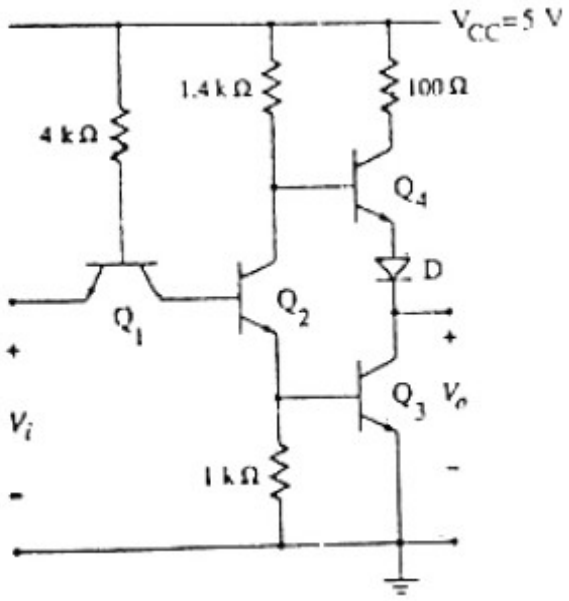
13. The Boolean function Y=AB+CD is to be realized using only 2-input NAND gates. The minimum number of gates required is

A) 2 B) 3 C) 4 D) 5

13. The Boolean Expression Y=A'B'C'D+A'BCD'+AB'C'D+ABC'D' can be minimized to

A)Y=A'B'C'D+A'BC'+AC'D B)Y=A'B'C'D+BCD'+AB'C'D
C)Y=A'BCD'+B'C'D+AB'C'D D) Y=A'BCD'+B'C'D+ABC'D'

14.The circuit diagram of a standard TTL NOT gate is shown in figure. When V1 =2.5 V,the modes of operation of the transistor will be



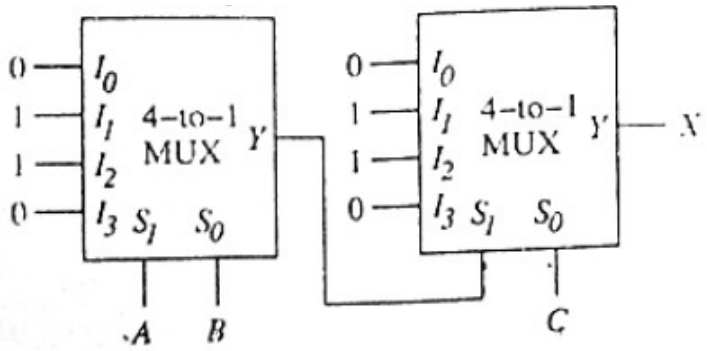
A) Q1: reverse active Q2: normal active Q3: saturation Q4: cut-off

B) Q1: reverse active Q2: saturation Q3: saturation Q4: cut-off

C) Q1: normal active Q2: cut-off Q3: cut-off Q4: saturation

D) Q1: saturation Q2: saturation Q3 saturation: Q4: normal active

15. The following circuit X is given by



a)X=AB’C’+A’BC’+A’B’C+ABC

b) X=A’BC+AB’C+ABC’+A’B’C’

c)X=AB+BC+AC

d) X=A’B’+B’C’+A’C’

(11) TUTORIAL QUESTIONS:

(12) SEMINAR TOPICS:

BCD to gray code converter

Digital Oscilloscopes

Logic gates emulator

The bio chips

Air Brake System

13. Objective questions:

1.What is the base for the octal [ ]

a) 2
b) 6
c) 7
d) 9

2. What is the equivalent binary number for Hexadecimal A

a) 1011
b) 1001
c) 0111
d) 1111

3.What is the range of decimal numbers

a) 1-10
b) 0-10
c) 1-9
d) 0-9

4.Binary Cell stores ___ numbers

a) only Binary numbers

b) Decimal

c) Ocatl

d) d)none

5.Excess-3 code is_____

a) adds 3

b) Subtract-3

c) Multiplies 3

d) none

6.Excess-3 code for 1011 is

a) 1110

b) 1010

c) 100000

d) none

7.Gray code for decimal 9 is

a) 1100

b) 1101

c) 1001

d) none

8.What is the range of BCD code

a) 0-15

b) 0-8

c) 0-9

d) none

9.The equivalent gray code of the following binary number is 1011100010

a) 1110010011

b) 1110010011

c) 1011

d) none

10.The equivalent binarycode for the following gray code is 101011

a) 101011

b) 110010

c) 101101

d) 110110

11.What is the equivalent decimal code for (237)8

a) 159

b) 160

c) 280

d) 789

12. What is the equivalent decimal code for (A3B)16

a) 2389

b) 2619

c) 654

d) 1234

13. What is the equivalent decimal code for (101111)2

a) 234

b) 567

c) 47

d) 87

14. What is the equivalent Binary code for (53)10

a) 110101

b) 11011

c) 1011

d) 110011

15. What is the equivalent octal code for (12.0625)10

a) 14.04

b) 378.8

c) 234

d) none

16. What is the equivalent Hexadecimal code for (250.5)10

a) AB56

b) FA.8

c) 270.9

d) 1189.3

17.Addition of 1111 and 1010 is ___

a) 11001

b) 110110

c) 1100

d) 1110

18.Subtraction of 111 and 1010

a) 101

b) 1000

c) 111

d) none

19.The 2's complement value for 10110 is

a) 01110

b) 01010

c) 1110

d) 1111

20 The 1's complement value for 10110 is

a) 01001

b) 11011

c) 11001

d) 1111

21.10’s complement value for 72546 is

a) 27453
b) 27454
c) 23456
d) none

22.9’s complement value for 72546 is

a) 27453
b) 27454
c) 23456
d) none

23.Register stores _____

a) 1 bit
b) group of bits
c) 5 bits
d) 8 bits

24.the 8421 code for 9 is

a) 1001
b) b)1010
c) 1000
d) none

25.The 9;s complement form is

a) (r^n+1)
b) $(r^n-1)\_N$
c) $(r^n-1)-N$
d) None

26. Which of the following is the same as its 2'S complement
A) 1010 B) 0101 C) 1000 D) 1001

27. Which gate is used to convert Gray code into Binary Code
A) NAND B) NOR C) EX-OR D) EX-NOR

28. In any number system Radix is
A) Odd number
B) Even number
C) Prime number
D) Real number

29. For n-bit Gray code we can generate how many bits reflected code
A) n^2 -bits
B) (n+1)-bits
C) (n-1)-bits
D) n-bits

30.For error detection and correction which of the following code is used
A) Parity bit B) ASCII code
C) Hamming code D) Hollerith code

31. The Max term corresponding 15 is
A) ABCD B) A'B'C'D'
C) A+B+C+D D) A'+B'+C'+D'

32. Essential prime implicates means
A) It is repeated in PI
B) It is not repeated in PI
C) At least one variable is not repeated in PI
D) None

33. A Demultiplexer can be used to realize a
A) Counter
B) Shift register
C) Combinational circuit
D) Display system

34. Which of the following device is used to convert serial data into parallel data
A) DMUX
B) MUX
C) Decoder
D) Encoder

35. Which of the following is Cyclic code
A) Gray code
B) Excess-3 code
C) BCD code
D) Hamming code

36. The master slave circuit is present in _____ flipflop
(a) J - K (b) R – S (c) T (d) All the above

37. A function table is required in very large numbers. The memory most suitable for this purpose is
(a) EPROM (b) EAROM (c) ROM (d) PROM

38. Which of these statements is true
(a) All logic functions are linearly separable
(b) Unate functions are necessarily linearly separable functions
(c) Threshold functions are linearly separable
(d) Unate functions are never linearly separable functions

39. In a counter consisting of four JK flip flops, all the flip flops get triggered simultaneously.
This counter circuit is
(a) Is an asynchronous circuit (b) Is a synchronous circuit
(c) Is a combinational circuit (d) May be combinational or sequential circuit

40. A sequential circuit with m flip flops and n inputs needs rows in the state table.
(a) 2m-n-1 (b) 2n (c) 2m+n (d) 2m

41. The number of directed arcs emanating from any state in a state diagram is
(a) 2n, where n is the number of inputs (b) an arbitrary number
(c) 2n, where n is number of flip flops in the circuit
(d) independent of the number of inputs

42. The basic flip-flops are
(a) J - K (b) R - S (c) T (d) All the above

43. Moore type of outputs are
(a) Dependent only on the inputs (b) Depends on the type of hardware used for implementation
(c) Independent of the inputs (d) Dependent on present state and input

44. An ASM chart of the mealy model
(a) Contains only state and decision boxes
(b) Contains conditional output box
(c) Does not contain conditional output box
(d) Outputs are represented writing output state variable inside state box

45. The control system fading of a digital system is
(a) Very simple circuit (b) Non linear circuit
(c) Only combinational circuit (d) Sequential circuit